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EXAMINER	
CHU, CHRIS C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/909,181	FARRAR, PAUL A.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 6, 2003 has been entered. An action on the RCE follows.

2. Applicant's amendment filed on May 6, 2003 has been received and entered in the case.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 ~ 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada in view of Hiraoka et al.

Regarding claim 1, Asada discloses in Fig. 8B a high density semiconductor structure having a plurality of integrated circuit chips, comprising:

- a first integrated circuit chip (131) having an upper bonding surface;
- a second integrated circuit chip (132) secured to the first chip in a manner such that a lower bonding surface of the second chip is positioned adjacent to the upper bonding surface of the first chip; and
- a chip insulating layer (601) disposed between the first and second chips so as to provide electrical isolation between the chips, wherein the chip insulating layer comprises an insulating material.

Asada does not disclose the chip insulating layer comprising a plurality of enclosed regions of air dispersed within and throughout the insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. However, Hiraoka et al. discloses in Fig. 1 a chip insulating layer (1) comprising a plurality of enclosed regions of air (2) dispersed within and throughout an insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Asada by using the plurality of enclosed regions of air into the chip insulating layer as taught by Hiraoka et al. The ordinary artisan would have been motivated

to modify Asada in the manner described above for at least the purpose of providing a plurality of regions formed in the insulating layer (column 5, lines 44 and 45).

Regarding claim 2, Asada discloses in Fig. 8B a conductor insulating layer (621) formed on the upper bonding surface of the first chip, wherein the conductor insulating layer provides electrical isolation between adjacent conductive leads (611a and 611j) disposed on the upper bonding surface of the first chip, wherein the conductor insulating layer comprises an insulating material.

Asada does not disclose the conductor insulating layer comprising a plurality of enclosed regions of air dispersed throughout the insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. However, Hiraoka et al. discloses in Fig. 2 and Fig. 3 a plurality of enclosed regions of air (2) dispersed throughout an insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Asada by using the plurality of enclosed regions of air into the conductor insulating layer as taught by Hiraoka et al. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of providing a plurality of regions formed in the insulating layer (column 5, lines 44 and 45).

Regarding claims 3 and 4, Asada discloses in column 6, lines 47 ~ 51 the chip insulating layer comprising a foamed polymeric material.

Regarding claim 5, Asada discloses in column 6, lines 47 ~ 51 the foamed polymeric material comprising a foamed polyimide.

Regarding claim 6, Asada discloses the claimed invention except for the foamed polyimide being approximately 2.1 microns thick. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use approximately 2.1 microns thick for the foamed polyimide, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of decreasing the device height.

Regarding claim 7, Asada discloses the claimed invention except for the foamed polymeric material comprising a hydrophobic material wherein the hydrophobic material is treated so as to provide the material with hydrophilic properties. However, it is well known in the art to use hydrophobic material for polymeric material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use hydrophobic material for polymeric material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of decreasing wiring capacity.

Regarding claim 8, Asada discloses the claimed invention except for the foamed polymeric material comprising polynorbornene. However, it is well known in the art to use polynorbornene for polymeric material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use polynorbornene for polymeric material, since

it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of increasing speed of operation.

Regarding claims 9 and 10, Asada discloses the claimed invention except for each enclosed region of air being approximately 0.1 micron. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use approximately 0.1 micron for each enclosed region of air, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of decreasing the device height.

Regarding claim 11, Asada discloses in Fig. 8B each enclosed region of air being less than the minimum distance separating adjacent conductive leads.

Regarding claim 12, Asada discloses the claimed invention except for the dielectric constant of the chip insulating layer being approximately one third of the dielectric constant of the insulating material. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use approximately one third of the dielectric constant of the insulating material to be the dielectric constant of the chip insulating layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The

ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of increasing operation speed.

Regarding claim 13, Asada discloses the claimed invention except for the dielectric constant of the insulating layer being less than 1.5. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use less than 1.5 dielectric constant for the insulating layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of increasing operation speed.

Regarding claim 14, Asada discloses the claimed invention except for the conductive leads being made of an aluminum alloy. However, it is well known in the art to use aluminum alloy for the conductive leads. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use aluminum alloy for the conductive leads, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of increasing corrosion-resistant.

Regarding claim 15, Asada discloses in Fig. 8B a third integrated circuit chip (133) wherein the third chip is secured to the second chip in a manner such that a lower surface of the third chip is positioned adjacent an upper surface of the second chip wherein a third insulating layer (602) is disposed between the second and third chips.

Regarding claim 16, Asada discloses in column 6, lines 47 ~ 51 the third insulating layer comprising a foamed polymeric material.

Regarding claim 17, Asada discloses in Fig. 8B the first integrated circuit chip further comprising a lower surface wherein a fourth insulating layer (16) is formed on the lower surface of the first chip.

Regarding claim 18, since Asada does not limit the fourth insulating layer to any particular or specific material, hence his/her disclosure encompasses all well known material including "foamed polymeric material."

Regarding claim 19, Asada discloses in Fig. 8B a multichip cube structure having a plurality of integrated circuit chips, comprising:

- a first integrated circuit chip (131) having a first insulating layer (621) disposed on an upper surface of the chip so as to electrically isolate a plurality of metal leads disposed on the upper surface thereof, wherein the first insulating layer is comprised of an insulating material having a first dielectric constant;
- a second integrated circuit chip (132) secured to the first chip in a manner such that a lower surface of the second chip is positioned adjacent the upper surface of the first chip;
- a second insulating layer (601) disposed between the first and second chips wherein the second insulating layer is comprised of a second insulating material having a second dielectric constant.

Asada does not disclose at least a portion of the first and second insulating layers containing a plurality of enclosed regions of air formed within the first and second insulating

material, the dielectric constant of the first insulating layer being lower than the first dielectric constant and the dielectric constant of the second insulating layer being lower than the second dielectric constant. However, Hiraoka et al. discloses in Fig. 1 at least a portion of the insulating layer (1) containing enclosed regions of air (2) formed within a insulating material, the dielectric constant of the first insulating layer being lower than the first dielectric constant and the dielectric constant of the second insulating layer being lower than the second dielectric constant. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Asada by using the enclosed regions of air as taught by Hiraoka et al. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of providing a plurality of regions formed in the insulating layer (column 5, lines 44 and 45).

Regarding claim 20, Asada discloses in column 13, lines 30 ~ 46 the first insulation material comprising a polymeric material.

Regarding claim 21, the limitation "the polymeric material is treated with a supercritical fluid so as to produce the enclosed regions of the air in the material" is product-by-process claim, even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177**

USPQ 523; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 22, Asada discloses in Fig. 8B each enclosed region of air being less than the distance between adjacent metal leads on the upper surface of the first chip.

Regarding claim 23, Asada discloses in column 6, lines 47 ~ 51 the second insulating material comprising a polymeric material.

Regarding claim 24, Asada discloses in column 6, lines 47 ~ 51 the polymeric material being polyimide.

Regarding claim 25, Asada discloses the claimed invention except for the foamed polymeric material comprising polynorbornene. However, it is well known in the art to use polynorbornene for polymeric material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use polynorbornene for polymeric material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of increasing speed of operation.

Regarding claim 26, the limitation "the insulating material is treated with a hydrogen containing radical so as to make the surface more hydrophilic" is product-by-process claim, even

though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

5. Claims 1 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al. in view of Hiraoka et al.

Regarding claim 1, Bertin et al. discloses in Fig. 2 a high density semiconductor structure having a plurality of integrated circuit chips, comprising:

- a first integrated circuit chip (7) having an upper bonding surface;

- a second integrated circuit chip (12) secured to the first chip in a manner such that a lower bonding surface of the second chip is positioned adjacent to the upper bonding surface of the first chip; and
- a chip insulating layer (10) disposed between the first and second chips so as to provide electrical isolation between the chips, wherein the chip insulating layer comprises an insulating material.

Bertin et al. does not disclose the chip insulating layer comprising a plurality of enclosed regions of air dispersed within and throughout the insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. However, Hiraoka et al. discloses in Fig. 1 a chip insulating layer (1) comprising a plurality of enclosed regions of air (2) dispersed within and throughout an insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Bertin et al. by using the plurality of enclosed regions of air into the chip insulating layer as taught by Hiraoka et al. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of providing a plurality of regions formed in the insulating layer (column 5, lines 44 and 45).

Regarding claim 19, Bertin et al. discloses in Fig. 2 a multichip cube structure having a plurality of integrated circuit chips, comprising:

- a first integrated circuit chip (7) having a first insulating layer (10) disposed on an upper surface of the chip so as to electrically isolate a plurality of metal leads (9)

disposed on the upper surface thereof, wherein the first insulating layer is comprised of an insulating material having a first dielectric constant;

- a second integrated circuit chip (12) secured to the first chip in a manner such that a lower surface of the second chip is positioned adjacent the upper surface of the first chip;
- a second insulating layer (11) disposed between the first and second chips wherein the second insulating layer is comprised of a second insulating material having a second dielectric constant.

Bertin et al. does not disclose at least a portion of the first and second insulating layers containing a plurality of enclosed regions of air formed within the first and second insulating material, the dielectric constant of the first insulating layer being lower than the first dielectric constant and the dielectric constant of the second insulating layer being lower than the second dielectric constant. However, Hiraoka et al. discloses in Fig. 1 at least a portion of the insulating layer (1) containing enclosed regions of air (2) formed within a insulating material, the dielectric constant of the first insulating layer being lower than the first dielectric constant and the dielectric constant of the second insulating layer being lower than the second dielectric constant. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Bertin et al. by using the enclosed regions of air as taught by Hiraoka et al. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of providing a plurality of regions formed in the insulating layer (column 5, lines 44 and 45).

6. Claims 1 ~ 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al. in view of Farrar.

Regarding claim 1, Bertin et al. discloses in Fig. 2 a high density semiconductor structure having a plurality of integrated circuit chips, comprising:

- a first integrated circuit chip (7) having an upper bonding surface;
- a second integrated circuit chip (12) secured to the first chip in a manner such that a lower bonding surface of the second chip is positioned adjacent to the upper bonding surface of the first chip; and
- a chip insulating layer (10) disposed between the first and second chips so as to provide electrical isolation between the chips, wherein the chip insulating layer comprises an insulating material.

Bertin et al. does not disclose the chip insulating layer comprising a plurality of enclosed regions of air dispersed within and throughout the insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. However, Farrar discloses in Fig. 1B and column 8, lines 39 ~ 62 a chip insulating layer (116) comprising a plurality of enclosed regions of air (cells) dispersed within and throughout an insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Bertin et al. by using the plurality of enclosed regions of air into the chip insulating layer as taught by Farrar. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described

above for at least the purpose of providing an integrated circuit that has adequate mechanical integrity, as well as a relatively low dielectric constant (column 2, lines 33 ~ 34).

Regarding claim 2, Bertin et al. discloses in Fig. 2 a conductor insulating layer (6) formed on the upper bonding surface of the first chip, wherein the conductor insulating layer provides electrical isolation between adjacent conductive leads (9) disposed on the upper bonding surface of the first chip, wherein the conductor insulating layer comprises an insulating material.

Bertin et al. does not disclose the conductor insulating layer comprising a plurality of enclosed regions of air dispersed throughout the insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. However, Farrar discloses in Fig. 1B and column 8, lines 39 ~ 62 a plurality of enclosed regions of air (cells) dispersed throughout an insulating material, wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Bertin et al. by using the plurality of enclosed regions of air into the conductor insulating layer as taught by Farrar. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of providing an integrated circuit that has adequate mechanical integrity, as well as a relatively low dielectric constant (column 2, lines 33 ~ 34).

Regarding claims 3 and 4, Bertin et al. discloses in column 7, lines 56 the chip insulating layer comprising a foamed polymeric material.

Regarding claim 5, Bertin et al. discloses in column 7, lines 56 the foamed polymeric material comprising a foamed polyimide.

Regarding claim 6, Bertin et al. discloses the claimed invention except for the foamed polyimide being approximately 2.1 microns thick. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use approximately 2.1 microns thick for the foamed polyimide, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of decreasing the device height.

Regarding claim 7, Bertin et al. discloses the claimed invention except for the foamed polymeric material comprising a hydrophobic material wherein the hydrophobic material is treated so as to provide the material with hydrophilic properties. However, it is well known in the art to use hydrophobic material for polymeric material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use hydrophobic material for polymeric material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of decreasing wiring capacity.

Regarding claim 8, Bertin et al. discloses the claimed invention except for the foamed polymeric material comprising polynorbornene. However, it is well known in the art to use polynorbornene for polymeric material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use polynorbornene for polymeric material, since

it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of increasing speed of operation.

Regarding claims 9 and 10, Bertin et al. discloses the claimed invention except for each enclosed region of air being approximately 0.1 micron. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use approximately 0.1 micron for each enclosed region of air, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of decreasing the device height.

Regarding claim 11, Bertin et al., as modified, discloses each enclosed region of air being less than the minimum distance separating adjacent conductive leads.

Regarding claim 12, Bertin et al. discloses the claimed invention except for the dielectric constant of the chip insulating layer being approximately one third of the dielectric constant of the insulating material. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use approximately one third of the dielectric constant of the insulating material to be the dielectric constant of the chip insulating layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The

ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of increasing operation speed.

Regarding claim 13, Bertin et al. discloses the claimed invention except for the dielectric constant of the insulating layer being less than 1.5. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use less than 1.5 dielectric constant for the insulating layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of increasing operation speed.

Regarding claim 14, Bertin et al. discloses the claimed invention except for the conductive leads being made of an aluminum alloy. However, it is well known in the art to use aluminum alloy for the conductive leads. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use aluminum alloy for the conductive leads, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of increasing corrosion-resistant.

Regarding claim 15, Bertin et al. discloses in Fig. 2 and Fig. 5 a third integrated circuit chip (a third chip from the right of c) wherein the third chip is secured to the second chip in a manner such that a lower surface of the third chip is positioned adjacent an upper surface of the second chip wherein a third insulating layer is disposed between the second and third chips.

Regarding claim 16, Bertin et al. discloses in column 5, lines 60 ~ 61 the third insulating layer comprising a foamed polymeric material.

Regarding claim 17, Bertin et al. discloses in Fig. 5 the first integrated circuit chip further comprising a lower surface wherein a fourth insulating layer (CP) is formed on the lower surface of the first chip.

Regarding claim 18, since Bertin et al. does not limit the fourth insulating layer to any particular or specific material, hence his/her disclosure encompasses all well known material including "foamed polymeric material."

Regarding claim 19, Bertin et al. discloses in Fig. 2 a multichip cube structure having a plurality of integrated circuit chips, comprising:

- a first integrated circuit chip (7) having a first insulating layer (10) disposed on an upper surface of the chip so as to electrically isolate a plurality of metal leads (9) disposed on the upper surface thereof, wherein the first insulating layer is comprised of an insulating material having a first dielectric constant;
- a second integrated circuit chip (12) secured to the first chip in a manner such that a lower surface of the second chip is positioned adjacent the upper surface of the first chip;
- a second insulating layer (11) disposed between the first and second chips wherein the second insulating layer is comprised of a second insulating material having a second dielectric constant.

Bertin et al. does not disclose at least a portion of the first and second insulating layers containing a plurality of enclosed regions of air formed within the first and second insulating

material, the dielectric constant of the first insulating layer being lower than the first dielectric constant and the dielectric constant of the second insulating layer being lower than the second dielectric constant. However, Farrar discloses in Fig. 1B and column 8, lines 39 ~ 62 at least a portion of the insulating layer (116) containing enclosed regions of air (cells) formed within a insulating material, the dielectric constant of the first insulating layer being lower than the first dielectric constant and the dielectric constant of the second insulating layer being lower than the second dielectric constant. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Bertin et al. by using the enclosed regions of air as taught by Farrar. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of providing an integrated circuit that has adequate mechanical integrity, as well as a relatively low dielectric constant (column 2, lines 33 ~ 34).

Regarding claim 20, Bertin et al. discloses in column 5, lines 60 ~ 61 the first insulation material comprising a polymeric material.

Regarding claim 21, the limitation "the polymeric material is treated with a supercritical fluid so as to produce the enclosed regions of the air in the material" is product-by-process claim, even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re

Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 22, Bertin et al., as modified, discloses each enclosed region of air being less than the distance between adjacent metal leads on the upper surface of the first chip.

Regarding claim 23, Bertin et al. discloses in column 5, lines 60 ~ 61 the second insulating material comprising a polymeric material.

Regarding claim 24, Bertin et al. discloses in column 5, lines 60 ~ 61 the polymeric material being polyimide.

Regarding claim 25, Bertin et al. discloses the claimed invention except for the foamed polymeric material comprising polynorbornene. However, it is well known in the art to use polynorbornene for polymeric material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use polynorbornene for polymeric material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. The ordinary artisan would have been motivated to modify Asada in the manner described above for at least the purpose of increasing speed of operation.

Regarding claim 26, the limitation "the insulating material is treated with a hydrogen containing radical so as to make the surface more hydrophilic" is product-by-process claim, even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Response to Arguments

7. Applicant's arguments with respect to claims 1 and 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
July 3, 2003